AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

Claims 1-86 (Canceled).

87. (Currently amended) A method of forming a structure for supporting an integrated circuit chip, which chip may be affected by external magnetic fields, said method comprising:

forming a substrate;

forming an insulating layer over said substrate;

providing a support surface for an integrated circuit chip, said substrate, insulating layer and support surface forming part of a chip carrier; and

supporting an integrated circuit chip with said chip carrier, said chip carrier having a top and bottom surface, wherein a layer of magnetic field shielding material is formed on said integrated circuit chip, and wherein a second layer of magnetic field shielding material is formed on a bottom of said chip.

88. (Previously presented) The method of claim 87, further comprising providing a second layer of magnetic field shielding material on top of said chip carrier.

89. (Previously presented) The method of claim 87, further comprising providing a second layer of magnetic field shielding material embedded within said substrate of said chip carrier.

90. (Previously presented) The method of claim 87, further comprising providing a second layer of magnetic field shielding material embedded within a printed circuit board electrically coupled to said chip carrier.

91. (Original) The method of claim 87, wherein said semiconductor device is a magnetic memory device.

92. (Original) The method of claim 91, wherein said magnetic memory device is a magnetic random access memory device.

93. (Original) The method of claim 87, wherein said layer of magnetic field shielding material comprises a magnetic material selected from the group consisting of ferrites, manganites, chromites and cobaltites.

94. (Original) The method of claim 93, wherein said magnetic material comprises MFe_2O_4, wherein M is at least one atom selected from the group consisting of Mn, Fe, Co, Ni, Cu, and Mg.

95. (Original) The method of claim 93, wherein said magnetic material comprises a material which includes conductive particles.

96. (Original) The method of claim 95, wherein said conductive particles are selected from the group consisting of nickel particles, iron particles, and cobalt particles.

97. (Canceled).

98. (Previously presented) The method of claim 87, further comprising providing a second layer of magnetic field shielding material on the bottom surface of said chip carrier.

99. (Currently amended) The method of claim [[97]] 87, further comprising providing a second layer of magnetic field shielding material on the top surface of said chip carrier.

100. (Currently amended) A method of forming a structure for supporting an integrated circuit chip, which chip may be affected by external magnetic fields, said method comprising:

forming a substrate;

forming an insulating layer over said substrate;

forming an elastomeric layer over said insulating layer, said substrate, insulating layer, and elastomeric layer forming part of a flip-chip carrier; and

electrically coupling a chip with said flip-chip carrier, said chip having a top and bottom surface, wherein said chip further comprises a layer of magnetic field shielding material formed on said top surface, and wherein a second layer of magnetic field shielding material is provided on the bottom surface of said chip.

101. (Canceled).

102. (Previously presented) The method of claim 100, further comprising a second layer of magnetic field shielding material provided between said substrate and said insulating layer.

103. (Previously presented) The method of claim 100, further comprising a printed circuit board electrically coupled to said substrate, said printed circuit board having a top and bottom surface.

104. (Previously presented) The method of claim 103, further comprising a second layer of magnetic field shielding material provided on said top surface of said printed circuit board.

105. (Previously presented) The method of claim 103, further comprising a second layer of magnetic field shielding material provided on said bottom surface of said printed circuit board.

106. (Previously presented) The method of claim 103, further comprising a second and third layer of magnetic field shielding material provided on said top and bottom surface of said printed circuit board.

107. (Previously presented) The method of claim 103, further comprising a second layer of magnetic field shielding material embedded within said printed circuit board.

108. (Previously presented) The method of claim 87, wherein said substrate comprises a flexible tape.

109. (Previously presented) The method of claim 87, wherein said substrate is a polyimide tape.

110. (Previously presented) The method of claim 100, wherein said elastomeric layer comprises silicone.

111. (Previously presented) The method of claim 110, wherein said elastomeric layer comprises a silicone-modified epoxy.

112. (Previously presented) The method of claim 100, further comprising forming conductive traces within said insulating layer.

113. (Previously presented) The method of claim 100, further comprising forming conductive traces between said insulating layer and said elastomeric layer.

114. (Previously presented) The method of claim 87, further comprising forming conductive traces within said insulating layer.

115. (Previously presented) The method of claim 87, further comprising forming conductive traces between said insulating layer and said support surface.

116. (New) A method of forming a structure for supporting an integrated circuit chip, which chip may be affected by external magnetic fields, said method comprising:

forming a substrate;

forming an insulating layer over said substrate;

providing a support surface for an integrated circuit chip, said substrate, insulating layer and support surface forming part of a chip carrier; and

supporting an integrated circuit chip with said chip carrier, said chip carrier having a top and bottom surface, wherein a layer of magnetic field shielding material is formed on said integrated circuit chip, and wherein a second layer of magnetic field shielding material is formed on said chip carrier.